REMARKS

Claim 1-14, 15-17, and 19-27 are pending in the application. No claims have been amended.

Rejection Under 35 U.S.C. §103(a)

The applicants' pending claims have been rejected over the Background section of the applicants' specification in view of Kim et al. This rejection is overcome in view of attached Declaration, together with the following remarks.

In their background section, the applicants describe the difficulty of integrating active and passive components. The applicants describe the problem that materials associated with passive components are often incompatible with processing requirements of active circuits. (Sub. Spec., pg. 1, beginning at line 23). Methods of the prior art using various capacitor dielectrics and perovskites are described. Methods of the prior art that seek to address the temperature incompatibility of dielectrics and metals interconnects are described. The applicants further describe the difficulty associated with the inability to vertically integrate active and passive components. (Sub. Spec., pg. 4, lines 27-30).

Another problem associated with integrating active and passive components relates to disturbance effects from the substrate used for the active components. (Sub. Spec., pg. 4, beginning at line 31). The applicants describe various solutions disclosed in the prior art to diminish disturbance effects. With respect to methods for reducing induced current caused by inductors and conductive lines, the applicants describe three know prior art solutions on page 5 of their Substitute Specification. One is to eliminate a portion of the substrate under areas in which inductors and conductive lines are formed. Another is to form insulation in areas that receive conductors and inductors. Yet another is to structure the underlying layers in a checkerboard pattern.

While the application describes various structures disclosed in the prior art, the claims are directed to an improved process for integrating the structures, and an improved device. Important advantages of the invention include implementation of a layer transfer technique. The applicants disagree with the Examiner's allegation that

the Background section of their specification sets forth or admits that the prior art discloses layer transfer. (Office Action, pg. 3). The applicants assert that nothing in the Background section of their specification suggests or discloses the layer transfer method recited in claim 1.

Further, the Examiner acknowledges that the applicants' Background section does not suggest or disclose "producing at least one interconnect line" as recited by claim 1. (Office Action, pg. 3). Kim et al. is cited as teaching the formation of an interconnect line between two substrates. The applicants assert that Kim et al. is not prior art to their invention. The applicants provide herewith a Declaration by Jean-Pierre Joly, a named inventor of the above-referenced application, that sets forth facts establishing prior conception of the subject matter disclosed by Kim et al. and relied upon by the Examiner.

As set forth in his Declaration, Mr. Joly states that before December 28, 2002, the earliest effective date of Kim et al., he received a draft French patent application from French patent counsel. The draft French patent application is attached to the Declaration as Exhibit A. Relevant portions of the draft French patent application are translated into English and are attached as Exhibit B. The formation of metal interconnects and other aspect of the claimed invention are disclosed in the draft French patent application.

Mr. Joly further states that with the assistance of his employer, the CEA, and French patent counsel, he and the co-inventors thereafter prepared revised drafts and diligently worked to file a French patent application on June 24, 2003.

The French application is application no. 0307617, which is the priority French application claimed in the applicants' corresponding PCT application no. PCT/FR04/01565.

The applicants assert that the Declaration and accompanying document establishes their prior conception any subject matter of Kim et al. considered relavant to their claimed invention. Accordingly, Kim et al. should be removed.

Kim et al. was first cited by the Examiner in the instant Office Action. Accordingly, in accordance with 37 C.F.R. §1.116(e), the applicants request entry and consideration of the accompanying Declaration. Should the Examiner find that the applicants' response does not place the application in condition for allowance, the Examiner is requested to contact the undersigned attorney by telephone at the number listed below.

The applicants have made novel and non-obvious contribution to the art of integrated circuits including active and passive components and to their fabrication. The claims at issue are distinguished over the cited references and are in condition for allowance. Accordingly, such allowance is now earnestly requested.

Respectfully submitted,

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